



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,005	12/01/2003	Crocifisso Marco Antonio Renna	2110-91-3	2701

7590 10/18/2005
GRAYBEAL JACKSON HALEY LLP
Suite. 350
155-108th Avenue N.E.
Bellevue, WA 98004-5973

EXAMINER

HARRISON, MONICA D

ART UNIT	PAPER NUMBER
----------	--------------

2813

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/726,005

Applicant(s)

RENNA ET AL.

Examiner

Monica D. Harrison

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) 18-40 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 and 41-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2003 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Claims 18-40 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 7/28/05.

Response to Arguments

2. In response to applicant's arguments, the apparatus and method of said claims are classified in separate statutory classes of inventions and the examiner has determined the separate class search is burdensome.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 and 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Murphy et al (US 2004/0142542 A1).

3. Regarding claim 1, Murphy et al discloses a SOI-type semiconductor substrate comprising at least a buried insulating cavity formed according to the following steps: form on said semiconductor substrate (Figure 1, reference 1) a plurality of trenches (Figure 1, reference 2), form a surface layer on said semiconductor substrate in order to close superficially said

Art Unit: 2813

plurality of trenches (Figure 1, reference 4) forming, in the meantime, said at least one cavity buried in correspondence with the surface-distal end of said trenches (Figure 1, reference 3); form a first semiconductor material layer on said surface layer with the same concentration as said semiconductor substrate wherein at least a trench is formed which is in communication with said at least one buried cavity (Figure 1, reference 5).

4. Regarding claim 2, Murphy et al discloses wherein said surface layer is formed through an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate (pg.3, paragraph 0041; pg.4, paragraphs 0048 and 0051)

5. Regarding claim 3, Murphy et al discloses wherein said surface layer is formed by means of a semiconductor material surface layer formed in the substrate (pg.3, paragraph 0044).

6. Regarding claim 4, Murphy et al discloses wherein said semiconductor material surface layer is formed on the substrate through epitaxy (pg.3, paragraph 0043; pg.4, paragraph 0050).

7. Regarding claim 5, Murphy et al discloses wherein said first semiconductor material layer is formed through epitaxy (pg.4, paragraph 0050).

8. Regarding claim 9, Murphy et al discloses a suspended membrane formed on a semiconductor substrate of a first type of concentration and comprising at least a buried insulating cavity formed through the following steps: form on said semiconductor substrate (Figure 1, reference 1) a plurality of trenches (Figure 1, reference 2), perform an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate (pg.4, paragraph 0048) up to form a surface layer on said semiconductor substrate in order to close superficially said plurality of trenches (Figure 1, reference 4) forming in the meantime said at least one buried cavity in

Art Unit: 2813

correspondence with the surface-distal end of said trenches (Figure 1, reference 3), said surface layer forming said membrane (Figure 1, reference 4).

9. Regarding claim 10, Murphy et al discloses wherein a first semiconductor material layer is formed on said surface layer with different concentration with respect to said semiconductor substrate (Figure 1, reference 5; pg.3, paragraph 0044).

10. Regarding claim 11, Murphy et al discloses wherein said first layer is an epitaxial layer (pg.3, paragraph 0043, pg.4, paragraph 0050).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-8, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al (2004/0142542 A1) in view of Komuro et al (5,322,811).

11. Murphy et al discloses all above claimed subject matter except the porous silicon (claims 6-8, 12, and 13).

Komuro et al discloses porous silicon (Figure 11A, reference 61; column 9, lines 29-35).

Since Murphy et al and Komuro et al are both from the same field of endeavor, the purpose disclosed by Komuro et al would have been recognized in the pertinent art of Murphy et al.

Art Unit: 2813

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Murphy et al with the teachings of Komuro et al, for the purpose of creating a smooth surface silicon member.

Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al (2004/0142542 A1) in view of Komuro et al (5,322,811).

12. Regarding claims 14-17, Murphy et al discloses a MOSFET transistor integrated on a semiconductor substrate of a first type of concentration and comprising at least one buried insulating cavity formed through the following steps: form on said semiconductor substrate (Figure 1, reference 1) a plurality of trenches (Figure 1, reference 2), perform an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate (pg.4, paragraph 0048) up to form a surface layer on said semiconductor substrate in order to close superficially said plurality of trenches (Figure 1, reference 4) forming in the meantime said at least one buried cavity in correspondence with the surface-distal end of said trenches. However, Murphy et al does not disclose the channel region of said MOSFET transistor (claim 14-17) and the porous silicon (claim 17).

Komuro et al discloses the channel region of said MOSFET transistor (Figure 16, reference 810) and the porous silicon (Figure 11A, reference 61).

Since Murphy et al and Komuro et al are both from the same field of endeavor, the purpose disclosed by Komuro et al would have been recognized in the pertinent art of Murphy et al.

Art Unit: 2813

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Murphy et al with the teachings of Komuro et al, for the purpose of manufacturing a recording head with integrally housed functional elements.

13. Regarding claims 15, Murphy et al discloses wherein a first layer is formed on said surface layer with the same concentration of said semiconductor substrate (Figure 1, reference 5).

14. Regarding claims 16, Murphy et al discloses wherein said first layer is formed through epitaxy (pg.4, paragraph 0048).

Claims 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al (2004/0142542 A1) in view of Komuro et al (5,322,811).

15. Regarding claim 41, Murphy et al discloses a semiconductor structure, comprising: a first portion of a semiconductor substrate (Figure 1, reference 1) a cavity disposed in the first portion of the semiconductor substrate (Figure 1, reference 3); and a second portion of the semiconductor substrate disposed over the cavity (Figure1, reference 5). However, Murphy et al does not disclose a device disposed in the second portion of the semiconductor substrate (claim 41), transistor (claim 42) nor the transducer (claim 43).

Komuro et al discloses et al does not disclose a device disposed in the second portion of the semiconductor substrate (Figure 7), transistor (Figure 16, reference 810) nor the transducer (Figure 16, reference 805).

Since Murphy et al and Komuro et al are both from the same field of endeavor, the purpose disclosed by Komuro et al would have been recognized in the pertinent art of Murphy et al.

Art Unit: 2813

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Murphy et al with the teachings of Komuro et al, for the purpose of manufacturing a recording head with integrally housed functional elements.

Claims 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al (2004/0142542 A1) and Komuro et al (5,322,811) in view of Eriguchi et al (6,033,928).

16. Murphy et al and Komuro et al disclose all above claimed subject matter except the microphone (claim 44).

Eriguchi et al discloses a microphone (column 22, line 47).

Since Murphy et al, Komuro et al and Eriguchi et al are all from the same field of endeavor, the purpose disclosed by Eriguchi et al would have been recognized in the pertinent art of Murphy et al and Komuro et al.

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Murphy et al and Komuro et al with the teachings of Eriguchi et al, for the purpose of detecting a variation in capacitance between an electrode and substrate.

Claims 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al (2004/0142542 A1) in view of Komuro et al (5,322,811).

17. Murphy et al discloses a semiconductor structure, comprising; a first portion of a semiconductor substrate (Figure 1, reference 1); a dielectric layer disposed on the first portion of the semiconductor substrate and having a remnant of a cavity (Figure 1, reference 3); and a second portion of the semiconductor substrate disposed on the dielectric layer and being electrically insulated from the first portion of the semiconductor substrate (Figure 1, reference 5).

Art Unit: 2813

However, Murphy et al does not disclose a semiconductor device disposed in the second portion of the semiconductor substrate.

Kumoro et al discloses a semiconductor device disposed in the second portion of the semiconductor substrate (Figure 16, references 810 and 805).

Since Murphy et al and Komuro et al are both from the same field of endeavor, the purpose disclosed by Komuro et al would have been recognized in the pertinent art of Murphy et al.

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Murphy et al with the teachings of Komuro et al, for the purpose of manufacturing a recording head with integrally housed functional elements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

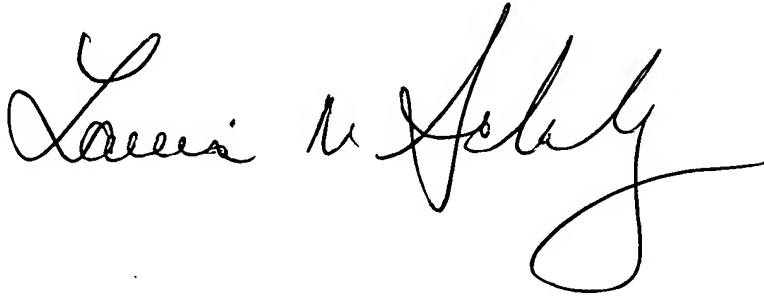
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2813

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
October 13, 2005

A handwritten signature in dark ink, appearing to read "Monica D. Harrison", with a large, stylized flourish at the end.